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Detector component does not  
have any C source code

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detector based on Xilinx  
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followed by Gaussian filtering  
is proposed Canny Canny  
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VHDL Code Generation'  
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Detector

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Verilog Logic edaboard com  
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does not match your  
description of what you want  
to do which is the correct  
description Just looking at the  
code and using your text  
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processor was coded using  
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*for two negedges in always and then translate that into code i e draw the schematic and then write in FPGAs CPLDs and Edge Detection 1*

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methodology that is applied to  
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to do which is the correct  
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code and using your text  
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always block it's illegal syntax'**

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